

In the Claims:

Please amend the claimed as indicated below.

1-5. (*Cancelled*)

6. (*Currently Amended*) An MIS type semiconductor device, comprising:

a semiconductor substrate,

a gate electrode formed on a gate insulating film and formed of gate material,

wherein the gate electrode comprises:

a first layer of activated crystalline gate material having a first side oriented towards the substrate and in contact with the gate insulating film, a second side oriented away from the substrate and a grain size, the first layer of activated crystalline gate material having a doping level of 10^{19} ions/cm³ or higher, and

a second layer of gate material in contact with the first layer of activated crystalline gate material at the second side of the first layer of activated crystalline gate material, the second layer of gate material having a grain size,

wherein the grain size of the second layer of gate material is at least twice as large as the grain size of the first layer of activated crystalline gate material.

7. (*Previously Presented*) A semiconductor device according to claim 6, wherein the first layer of activated crystalline gate material has a doping level of about 10^{20} ions/cm³ or higher.

8. (*Previously Presented*) An MIS type semiconductor device according to claim 6, wherein a doping implant in the activated gate material has an abruptness of a doping profile of about 2 nm or more.

9. (*Previously Presented*) A semiconductor device according to claim 6, wherein the second layer of gate material consists of amorphous gate material.

10. (*Previously Presented*) A semiconductor device according to claim 6, wherein the second layer of gate material consists of polycrystalline gate material.

11. *(Previously Presented)* A semiconductor device according to claim 6, wherein the grain size in the second layer is below about 40 nm.
12. *(Original)* A semiconductor device according to claim 6, wherein the first layer is crystalline or very fine-grained, with grains below 5 nm.
13. *(Currently Amended)* A semiconductor device according to claim 6, wherein the ~~[[a]]~~ gate insulating film ~~insulator~~ is provided between the semiconductor substrate and the gate electrode.
14. *(Original)* A semiconductor device according to claim 6, wherein the device is a transistor.
15. *(Cancelled)*
16. *(Cancelled)*
17. *(Previously Presented)* A semiconductor device according to claim 6, wherein the first layer of activated crystalline gate material has a doping level of about 5×10^{20} ions/cm³ or higher.
18. *(Previously Presented)* An MIS type semiconductor device according to claim 6, wherein a doping implant in the activated gate material has an abruptness of a doping profile of about 1.5 nm or more.
19. *(Previously Presented)* An MIS type semiconductor device according to claim 6, wherein a doping implant in the activated gate material has an abruptness of a doping profile of about 1 nm.

20. *(Previously Presented)* A semiconductor device according to claim 6, wherein the grain size in the second layer is below about 30 nm.

21. *(Previously Presented)* A semiconductor device according to claim 6, wherein the grain size of the second layer of gate material is about six times as large as the grain size of the first layer of activated crystalline gate material.

22. *(Previously Presented)* A semiconductor device according to claim 6, wherein the grain size of the first layer of activated crystalline gate material reduces gaps between the first layer of activated crystalline gate material and the gate insulating film.

23. *(Previously Presented)* A semiconductor device according to claim 6, wherein the first layer of activated crystalline gate material is silicon.

24. *(Currently Amended)* An MIS type semiconductor device, comprising:

- a semiconductor substrate;

- a gate insulating film formed on the substrate; and

- a gate electrode formed on the gate insulating film, the gate electrode including:

- a first layer of activated crystalline gate material having a first side oriented towards the substrate and in contact with the gate insulating film, a second side oriented away from the substrate and a grain size of less than about 5nm, the first layer of activated crystalline gate material having a doping level of 10^{19} ions/cm³ or higher, and

- a second layer of gate material in contact with the first layer of activated crystalline gate material at the second side of the first layer of activated crystalline gate material, the second layer of gate material having a grain size of less than about 40 nm,

- wherein the grain size of the first layer of activated crystalline gate material is smaller than the grain size of the second layer of gate material.